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Enhancement of minority carrier lifetime in low quality silicon by ion implantation of arsenic and antimony

by

Jason Edward Jirak

A thesis submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering

Program of Study Committee:
Vikram L Dalal, Major Professor
Mani Mina
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Iowa State University

Ames, Iowa

2009

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I dedicate this work to my wonderful wife, Michelle, for her support and patience.

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Abstract

The scope of this work is to determine the effect of ion implantation on the minority carrier lifetimes of upgraded metallurgical grade (UMG) silicon solar cells. Two species of atoms, arsenic and antimony, are used to getter impurities on P doped UMG wafers. The lifetimes of these wafers are measured before and after the implant process and after various annealing sequences using photoconductivity measurements provided by a Sinton WCT-120. Devices are then fabricated on these wafers so that lifetime trends measured by photoconductivity can be verified by reverse recovery time transient and quantum efficiency techniques. Ultimately, minority carrier lifetime measurements allow determination of the combination of implant species and annealing techniques that best increase the minority carrier lifetimes of the UMG wafers. Both arsenic and antimony implants proved capable of increasing minority carrier lifetime by a factor of ten.

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Chapter 1: Motivation

Solar photovoltaic electricity generation is a necessary technology needed to alleviate rising ratios of energy demand to generation and to combat the production of greenhouse gasses and other pollutants produced by hydrocarbon burning technologies. While solar cells provide an excellent solution to the world's current energy crisis, they have one fatal drawback: a low short-term profit to power production ratio. Improvement of this fundamental electrical energy generation method is being sought through several methods. The first, and most obvious, of these approaches is to increase the physical efficiency of the solar collecting devices themselves. Many times however, this is done at the expense of producing photovoltaic devices at greatly increased costs. Perhaps the most essential technique of increasing the profit to power ratio, is to decrease the fabrication and maintenance costs of the photovoltaic generator.

The primary material for creating photovoltaic generators is multicrystalline silicon which is produced from the scrap wafers of the electronic devices industry. Such materials have purities of 99.999999% (eight nines) to 99.9999999% (nine nines). Great expense is required to attain the high purities necessary to have a minimal number of electron and hole traps within the material. Due to the value-added nature of the products produced by the electronics industry, the cost of high purity raw materials is an afterthought. Unfortunately for the photovoltaic energy industry, which requires manufacturing solar cells by the square kilometer, material cost is of the utmost concern.

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There are two ways to address this problem; the first is to create solar cells which use little or no silicon. This is done using thin-film or organic technologies. The problems with these two technologies are shorter lifespan and lower efficiencies of devices compared to crystalline silicon. The other solution is to use a lower grade of silicon. Silicon is generally made from quartzite and is one of the most abundant materials within Earth's crust [1]. Costs associated with the high purity silicon required for the semiconductor industry are primarily attributed to the energy intensive purification process. If a lower quality of silicon was used, then the cost of silicon substrates could be greatly reduced.

A solar cell operates on by the following two processes: absorption of photons from incident light and collection of photo-induced charge carriers. First, light enters the cell where it is absorbed by the semiconductor lattice. Electron-hole pairs are created by the absorbed photons. Finally, the electron and hole need to flow to their respective contact points. Minority carrier diffusion length is a metric that describes how far the electron or hole can travel in a semiconductor material before it is trapped by a defect in the material. Minority carrier diffusion length is intimately related to the minority carrier lifetime. Increases in carrier lifetime increase the diffusion length in a given material.

For a solar cell, the purity of the silicon is not as important as the diffusion length of the charge carriers within the material. As long as the diffusion length and the photo-absorbance of the material are not terribly reduced, a high silicon purity level is not

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extremely critical. Upgraded metallurgical grade (UMG) silicon has similar properties to crystalline silicon, but its cost and purity are much lower.

One possible technique to improve the minority carrier lifetime and, as a result, the diffusion length of UMG is to engineer defects within the material. These defects, if properly manipulated, will act as impurity magnets which will adsorb the impurities thus providing trap-free paths for excitons. This trapping of impurities is called gettering. Lattice stress created by defect engineering will also improve carrier collection by improving mobility which is also intimately related to diffusion length. Ion implantation is a convenient method for creating layers with both gettering dopants and defects. Using ion implantation, both dopant and lattice defects can be accurately placed [2,3,4,5,6,7,8].

According to Siedel et. al. [2], implant species that cause more lattice damage should be able to provided better gettering. The difficulty is that the appropriate annealing technique has to be used to provide the appropriate amount of repair to lattice damage and to drive impurities to the gettering sites. The goal is to electrically de-activate any impurity that lies within the low grade silicon substrate near the location of the active pn junction. Phosphorous diffusion has been shown to provide excellent gettering of impurities with modest annealing temperatures (~1000 °C). Arsenic implant is comparable to phosphorous for high annealing temperatures [2]. Antimony is a larger atom than arsenic, so intuitively it could cause more lattice damage and therefore be an effective gettering species at even higher annealing temperatures.

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Chapter 2: Methodology

Ion Implantation

Ten 4 inch, P-type, UMG wafers of various types are sliced into quarters using a wafer dicing saw from MTI. The wafers are designated C2 through F3 by the manufacturer. Cuts are aligned normal to the wafer flat thus allowing two of the four wafer slices to be marked by the flat (See Figure 2.1). Wafer slices with the flat contained in their edges are set aside for ion implantation while the other two wafer slices are used for baseline reference and phosphorous diffusion.

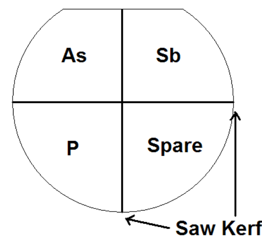

Figure 2.1 Wafer saw pattern

Ten wafer slices containing the flat in their edges are cleaned with boiling acetone followed by an RCA standard clean to remove all traces of the mounting wax used to saw the wafers. After such cleaning, the wafer slices are labeled with permanent marker and placed in two inch plastic jewel cases for shipping.

Core Systems Inc is contracted to perform both arsenic and antimony implantations. Both implantations are performed as separate orders, shipped several days

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apart to minimize any possibility of mix-up. Table 2.1 shows the implant parameters for both arsenic and antimony.

Table 2.1

	Arsenic	Antimony
Desired junction depth	500 nm	500 nm
Desired background concentration	$10^{19}cm^{-3}$	$10^{19}cm^{-3}$
Maximum implant energy	200 keV	190 keV
Implant dose	$10^{15}cm^{-2}$	$10^{15}cm^{-2}$

Implant energy and dose are selected from the following charts in Figure 2.2.

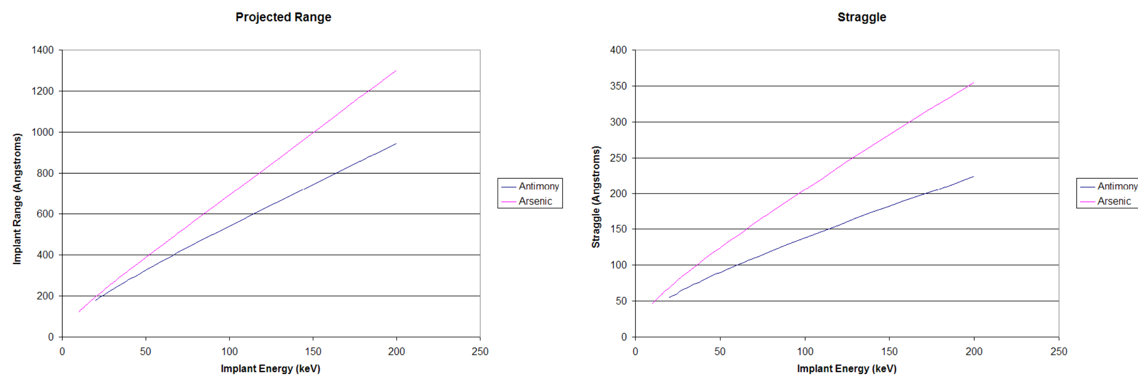

Figure 2.2 Plots of range and straggle versus energy [9].

Junction depth is used to determine range and hence implant energy. For this work the maximum implant energy for each dopant species is used to achieve sufficient depth. Once implant energies are determined, dose can be computed from Equation 2.1

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$$N(0) = \frac{Q}{\sqrt{\pi} R_P} \qquad (2.1)$$

Where N(0) is the surface concentration, Q is the implant dose, and R_P is the straggle at particular implant energy for a particular species of atom [10]. The implant angle for both arsenic and antimony wafer slices is set to 0 degrees. Core Systems calculates the necessary beam currents for their equipment based on the customer specified dose and implant energy.

Photoconductance Lifetime Measurements

Once the wafer slices reserved for implant are shipped, the remaining bare wafers are divided into two groups; one group is used for baseline measurement while the other group is used for conventional phosphorous diffusions. Initial lifetime measurements are made on the unprocessed wafers after the machining wax was removed with boiling acetone. A Sinton Consulting WCT 120 is used to make all preliminary minority carrier lifetime measurements. This apparatus operates on the principle of a time of flight experiment.

The apparatus consist of three primary components: a xenon flash lamp mounted on a stand, a sample platen containing a radio frequency (RF) assembly, and computer containing a National Instruments data acquisition card. The system is controlled through Microsoft Excel. The setup is shown in Figure 2.3.

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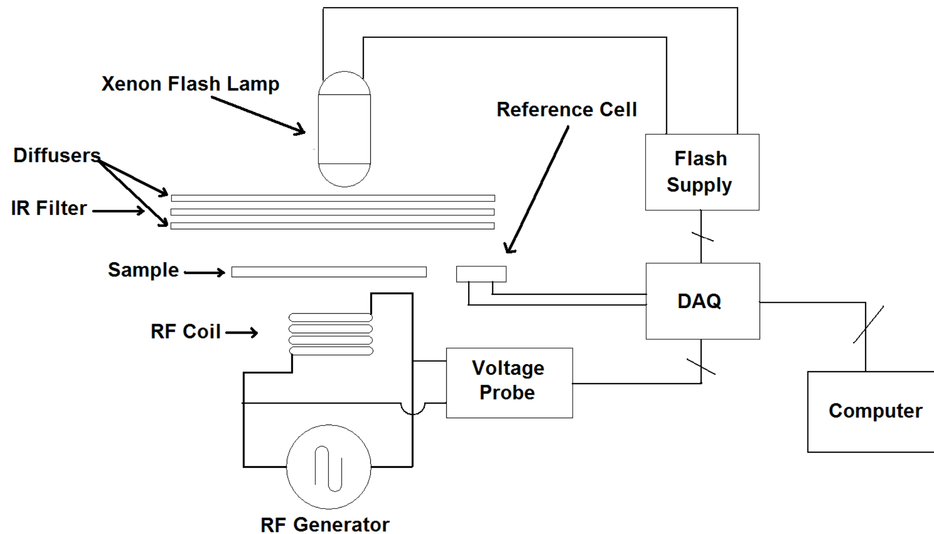

Figure 2.3 Block diagram of the Sinton apparatus

The fundamental operating principle of the machine is based on electromagnetic induction. A coil is mounted below the sample (wafer slice) as shown in Figure 2.3. The magnetic field created by the coil bathes the wafer slice. This magnetic field, which varies sinusoidally with time, creates a time varying electric field in the wafer slice. This electric field creates a current density which is proportional to resistivity as given by Ohm's law. The induced current density in the sample creates a magnetic field in the opposite direction as the coil field (Lenz's Law). This magnetic field acts on the coil, reducing its voltage drop. Reduction in coil voltage is linearly proportional to the conductivity of the wafer material. An equivalent circuit is show below in Figure 2.4.

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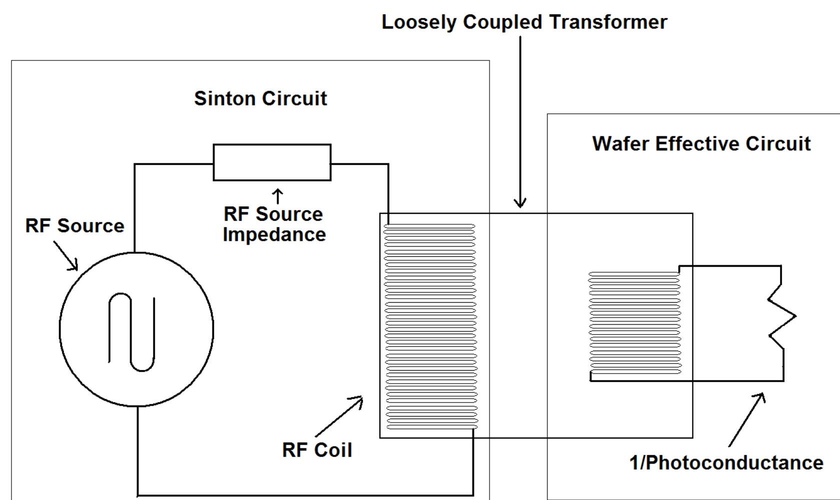

Figure 2.4 Equivalent circuit of RF conductance measurement

This RF sensing technique allows contactless photoconductance measurements of substrates. The xenon flash bulb provides the light pulse needed to create photo-induced carriers. A reference solar cell synchronizes the conductivity measurement with the light pulse (refer to Figure 2.3). Finally, the decay rate of the light pulse (reference solar cell voltage) is compare to that of the RF coil voltage to determine the carrier lifetime.

Hence this system is essentially the same as a typical laser based time of flight apparatus. One flaw that the WCT 120 possesses is the slow decay rate of the flash lamp. The flash lamp of the system is a basic photography flash lamp which is intended to illuminate objects for several milliseconds while an exposure is being taken for a photograph. Ideally, in a laser based time of flight measurement system, the duration of the light pulse will be at least two orders of magnitude less that the shortest minority carrier lifetime that is desired to be measured. Since the light pulse of the WCT 120 is on

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the same order of magnitude of the minority carrier lifetime, the lifetime is determined by the rate of decay of the photoconductivity compared with the rate of decay of the flash lamp.

All calculations are performed in an Excel spreadsheet supplied with the system. The basic software package allows for the calculation of minority carrier lifetime as a function of apparent carrier concentration the Auger corrected inverse carrier lifetime versus carrier concentration, and the apparent open circuit voltage. A calibration (zeroing of RF coil) is performed for each measurement. Optimum settings are obtained with the auto scaling feature of the software. Lifetime data is saved in its own spreadsheet.

Device Fabrication

Several solar cell devices were made by conventional phosphorous diffusion methods. A Thermco Brute furnace was restored and commissioned for the task. All boats were cleaned with a solution of hydrofluoric acid combined with nitric acid and de-ionized water (1:1:1). Caps and push rods were cleaned with a solution of hydrogen peroxide and sulfuric acid (1:1). Tubes are purged with dry nitrogen gas.

Fabrication of the diffused phosphorous solar cells begins with protecting both sides of the wafer slices with 200 nm of oxide. Wafer slices are first processed with the RCA standard clean (See Appendix I) to remove surface impurities; then oxide is grown via pyrolytic wet oxidation (See Appendix II). Slices are then stripped of the oxide on the front surface with buffered oxide etch (See Appendix II). Oxide is stripped by

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floating the slices on the surface of the etchant, thus eliminating the need to protect the back oxide with photoresist or wax.

Again wafer slices are processed through the RCA standard clean. Then the slices are placed adjacent to phosphorous source wafers. The phosphorous tube is ramped to its processing temperature and the phosphorous boat is then pushed to the center zone. Nominally the tube is ramped with the boat already in the center zone, but in the case of phosphorous, deposition occurs as soon as the wafers reach deposition temperature. Boron deposition and oxidation are controlled by the chemistry of the ambient gasses. Ambient used for all phosphorous depositions is dry nitrogen.

After soaking for the requisite time, the phosphorous boat is pulled out before the furnace tube is ramped down. The wafer slices are deglazed with buffered oxide etch. Completion of the deglazing step is determined by when the phosphorous exposed surface becomes hydrophobic. Another standard clean step is performed and the slices are oxidized and the phosphorous dopant is driven in. A background concentration of approximately $10^{19}cm^{-3}$ and a junction depth of 500 nm are the desired doping parameters.

With the N-type phosphorous dopant in place, the minority carrier lifetime of each phosphorous doped wafer slice is again measured with the Sinton WCT-120. Then the backside of each slice is stripped in the identical manner as the front side was previously. After appropriate cleaning the slices are placed adjacent to boron nitride

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source wafers and pushed into the boron tube. The tube is then ramped to deposition temperature and the recovery process is started. Recovery ambient consists of 1 SLPM of oxygen and 1 SLPM of nitrogen. After a 20 minute recovery, the boron is sourced by adding to the ambient mixture 200 SCCM of hydrogen. This gas is allowed to flow for 2 min before an ambient of 2 SLPM nitrogen is restored. During this period, boron soaks into the slices.

Following a predetermined soak period, the boron tube is ramped down to loading temperature and the boat is pulled out. Slices are deglazed for 2 minutes with buffered oxide etch to remove boron surface glass. Samples are then oxidized at 800 °C for 2 hours in an ambient of 500 SCCM oxygen to remove surface nitride. Once oxidation is complete, slices are again etched with buffered oxide etch for two minutes. Boron doped surfaces are hydrophobic once this process is complete.

Once the boron is diffused, aluminum contacts are applied to the front and back surfaces of the wafer slice. First, slices are dipped in buffered oxide etch to remove any remaining oxides. Slices are then immediately placed under vacuum in a Temescal 1800D electron beam evaporator. The evaporator is allowed to reach a pressure of 10^{-6} Torr. Once at pressure, 500 nm of aluminum are deposited at a rate of 4 angstroms per second. This procedure is repeated for the other side of the wafer slice.

With contact metal placed, AZ5214E photoresist is applied to both sides of the wafer slice. The backside is coated first with about 2 μm of resist and then baked for 30

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minutes at 80 °C. The front side is then spun with 2 μm of photoresist and also baked with the same parameters as the backside. A Karl Suss 3 inch mask aligner is used to apply the contact pattern as shown in Figure 2.5.

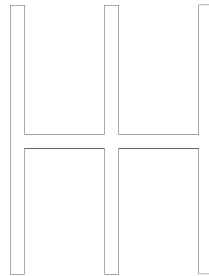

Figure 2.5 Contact pattern

Since the pattern is from a shadow mask, the exposure must is reversed. The reversal procedure used is to first expose with light; 360 mJ at 320 nm and 140 mJ at 365 nm. Next, the slices are baked for 2 minutes at 120 °C to cross link the exposed areas. Finally another light exposure is performed with the following optical parameters: 810 mJ at 320 nm and 180 mJ at 365 nm. Photoresist is now developed with MIF 300 developer (See Appendix II). Development typical takes 1 minute to complete. Slices are then baked at 120 °C for 1 hour to harden the photoresist.

Next, the slices are etched with a solution of phosphoric acid, acetic acid, nitric acid, and water (16:1:1:2) to remove unnecessary aluminum. Etching requires approximately four minutes for each slice. After etching, photoresist is removed by soaking slices in acetone for 60 minutes, rinsing in methanol for 1 minute and then de-ionized water for 3 minutes.

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To form solid ohmic contacts, the slices are sintered for 1 hour at 400 °C. This operation is performed in a spare tube in the Thermco furnace. Wafer slices are only cleaned in acetone and methanol as the RCA standard clean will compromise the metal contacts.

The final step to create a solar cell device is defining the emitter region. This is accomplished by masking a 1.25 by 1.25 cm area over each front contact using 3M vinyl electrical tape. Back contacts are also protected by electrical tape. Slices are then immersed for five minutes in a solution of hydrochloric acid and water (3:1) to remove any excess aluminum not covered by the tape. Next, the slices are rinsed with DI water and then immersed into a solution of hydrofluoric acid and nitric acid (1:10) for 1 minute to etch off approximately 5 microns of silicon from the surface, thus eliminating the entire exposed n-layer.

Device Characterization

Sample diode current- voltage (I-V) characteristics of each solar cell device are then measured with a HP 4156 parameter analyzer to determine the presence of excessive shunt resistance. If the shunt resistance is significantly greater than the series resistance, then the current- voltage (I-V) characteristics of each sample are measured under light from a GE ELH bulb. Light intensity is calibrated to 1 sun at the location of the solar cell device. This particular lamp is used for its close approximation to the spectrum of natural sunlight. Device bias voltage is provided by a Kepco bipolar operational power supply /

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amplifier. Bias voltage level is measured with a Keithly 177 multimeter. Current is measured with a different Keithly 177. Figure 2.6 schematically depicts the functional construction of the measurement apparatus.

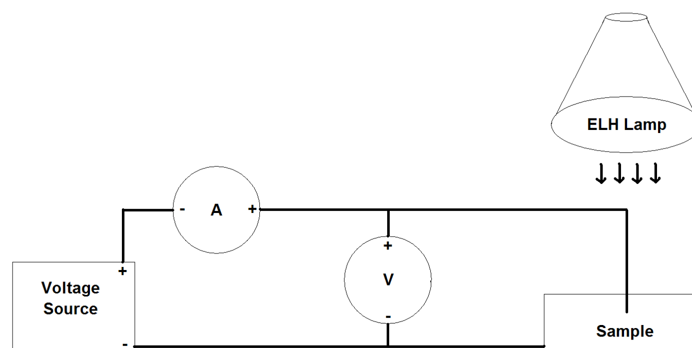

Figure 2.6 I-V measurement apparatus

Data from the I-V measurement are plotted in Excel. Figure 2.7 shows the typical shape for such a plot.

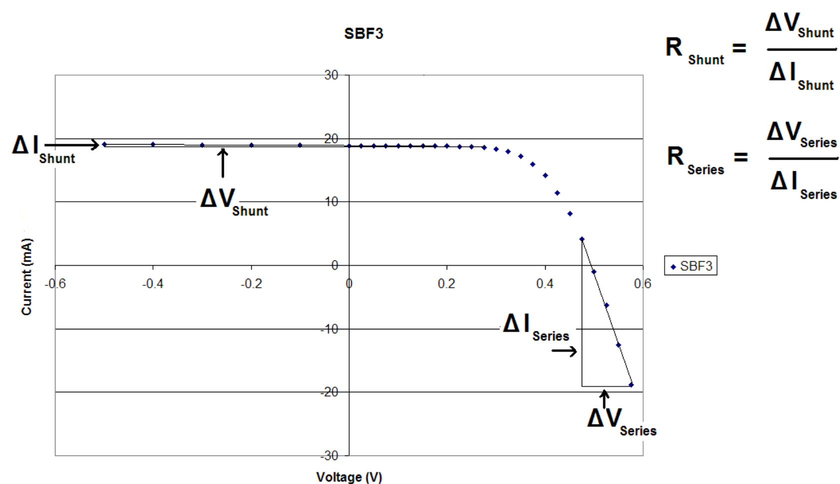

Figure 2.7 I-V curve

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Series resistance, fill factor, and shunt resistance are readily ascertained from this plot. Fill factor is calculated by dividing the maximum power by the product of short circuit current and open circuit voltage. Shunt resistance is determined from the reciprocal of the slope of the portion of the I-V curve located in quadrant two of the plot. Series resistance is determined from the reciprocal of the I-V curve located in quadrant four.

After obtaining the I-V characteristics of each measurable device (sample), the lifetime is measured by a reverse recovery transient technique (RRT). The experimental setup is demonstrated schematically in Figure 2.8.

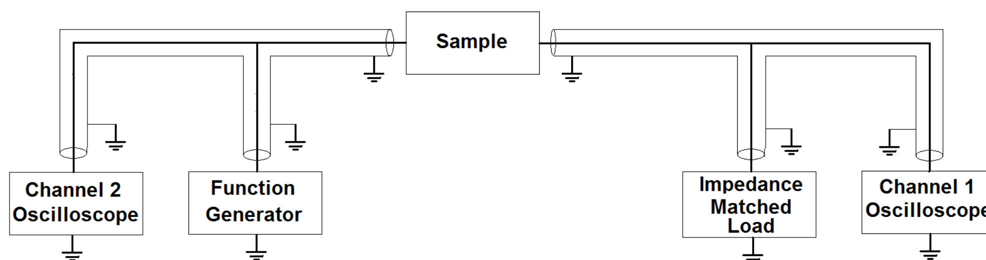

Figure 2.8 Experimental setup for RRT

The physical operating principle behind this measurement is that when a forward biased diode is thrown into reverse bias, current will still flow until the entire minority carrier population each electronic region of the diode recombines. This results in the waveform of Figure 2.9.

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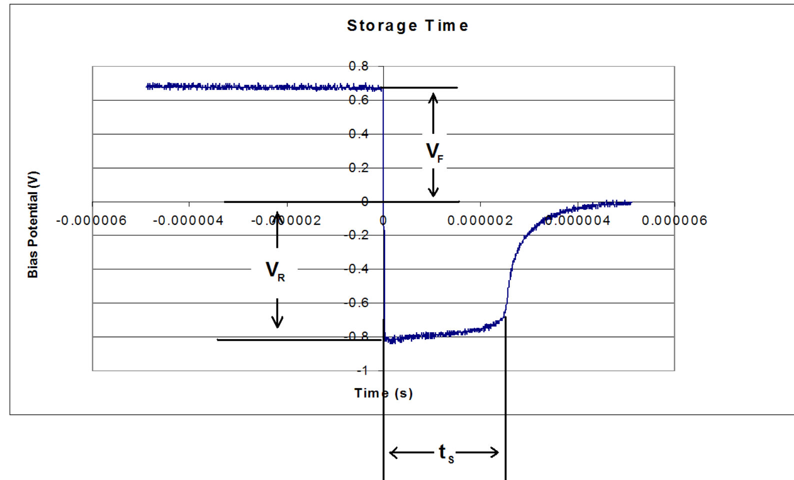

Figure 2.9 Typical RRT waveform

The flat portion of the curve seen just as the device goes into reverse bias is referred to as the storage time. Storage time is related to minority carrier lifetime by Equation 2.2

$$t_S = t_P \ln\left(1 + \frac{I_F}{I_R}\right) \tag{2.2}$$

where t_S is the storage time, t_P is minority carrier lifetime, I_F is forward current, and I_R is reverse current. Several values of storage time are measured for several different ratios of forward to reverse current. Data are plotted in Excel and the minority carrier lifetime is extracted from the slope of storage time versus the natural logarithm of the ratio of forward to reverse current plus one [11].

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Quantum efficiency of each device was measured with the apparatus schematically depicted in Figure 2.10.

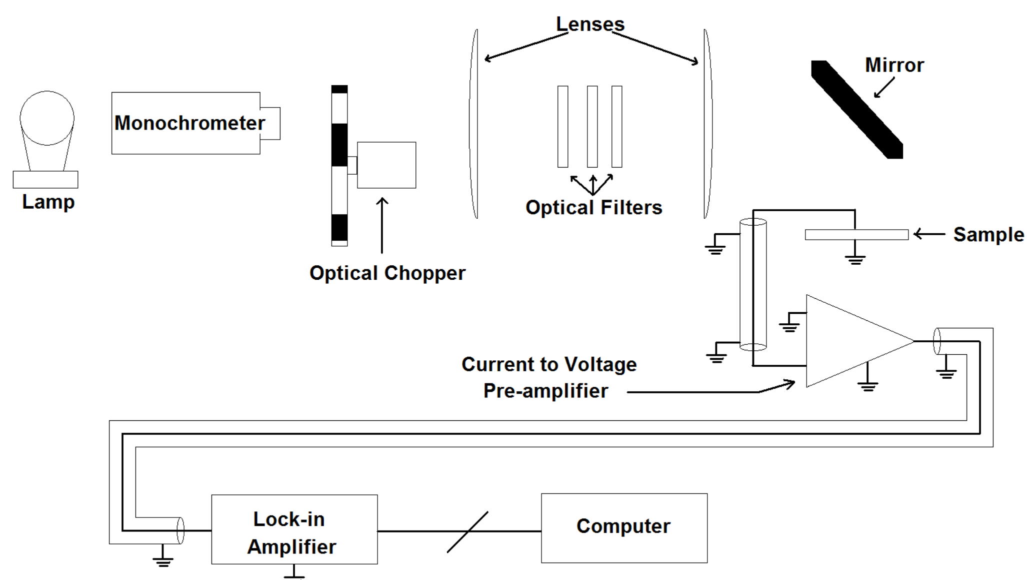

Figure 2.10 Quantum efficiency apparatus

The operation of this system is as follows. A chopped beam of light impinges on the device and creates an AC current signal. This signal is detected and converted to a voltage signal by a pre-amplifier, which feeds a Stanford Research Systems lock-in amplifier which passes the RMS value of the AC signal to a computer. The wavelength of the light is varied with a monochrometer from 400 to 1100 nm and the AC signal level is recorded as a function of the wavelength. A DC bias light is supplied to the sample with an ELH lamp. This bias light is used to stabilize the quasi Fermi levels during the measurement. The measured AC signal is compared to that of a crystalline silicon reference cell and normalized to 0.9.

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The purpose of the quantum efficiency measurement is to observe the spectral response of the solar cell. Quantum efficiency is also a vital parameter for determining the diffusion length. Diffusion length can be found using Equation 3.3

$$QE(\lambda) = (1 - R(\lambda))\frac{\alpha(\lambda)L_P(\lambda)}{1+\alpha(\lambda)L_P(\lambda)} \quad (2.3)$$

where QE is normalized quantum efficiency, R is reflectance of the silicon, α is the absorption coefficient of crystalline silicon, and L_P is the minority carrier diffusion length. This equation is only valid for in cases where $\alpha W_D << 1$. The term W_D is the depletion width and is found from Equation 2.4. This relation is only valid for lopsided junctions ($N_D >> N_A$) where N_D is the number of donor states and N_A is the number of acceptor states like those used for this work.

$$W_D = \sqrt{\frac{2\varepsilon(V_B - V_A)}{qN_A}} \quad (2.4)$$

where ε is the electric permittivity, V_B is the built in potential and V_A is the applied voltage. Using a maximum possible built in voltage of 1.2 V and the measured background doping of $3 \times 10^{16} cm^{-3}$ the depletion width is not going to exceed 220 nm, which is much less than the lowest diffusion length of 20 µm. At the wavelengths used to measure diffusion length the largest value of absorption coefficient is 300; hence, the product of absorption coefficient and depletion width are 0.001 which is much less than 1.

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Data for the absorption coefficient was obtained from a previous measurement on crystalline silicon. Similar data can also be obtained from on-line tables and calculator applications. Absorption coefficient is strongly dependant on optical wavelength, so values for each wavelength are needed.

Reflection versus wavelength is measured using an Ocean Optics HR4000. Quantum efficiency is divided by the transmittance (1-R) and plotted in the following manner: the quantity 1/QE versus 1/α. The reciprocal of the slope of this curve is equal to the minority carrier diffusion length provided the previously stated condition is met. Equation 2.5 relates the minority carrier diffusion length to the minority carrier lifetime.

$$\frac{D_P}{\mu_P} = \frac{k \cdot T}{q} \qquad (2.5)$$

Where D_P is the diffusion coefficient for holes, μ_P is the hole mobility, k is the Boltzman constant, T is the temperature, and q is the fundamental charge. For room temperature measurements and a hole mobility of 300 cm^2/Vs, D_P is 10 cm^2/s.

Devices made with arsenic and antimony ion implanted wafer slices are measured and prepared in a similar manner as those made using phosphorous. The primary differences are that the implanted ions served as the N-layer rather than phosphorous and the devices had only aluminum for the back contact as opposed to the P+ layer created

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during the boron doping stage. Aluminum can be used in place of boron as a P-type dopant provided that the annealing temperature is high enough ($T > 550$ °C) [12].

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Chapter 3: Data

Device Data

Throughout the remainder of this work, wafer slices are designated as follows, the first capital and small letter indicate the dopant species (P, As, Sb) and the next letter and numeral indicate the parent wafer (C2, C3, D2, D3, D4, E3, E4, E5, F2, F3) (See Table 3.1). Typically, in the literature, the implanted region of the solar cell is removed after the impurity gettering anneal step. After the implanted region is removed, the n+p junction is formed with conventional phosphorous diffusion. Solar cells made for this work however have their junctions directly formed from the gettering implant. Sixteen devices were made and six of these devices had fill factors greater than 58. Resulting device properties are shown below and substrate characterization is described later in this section.

The best devices are made by phosphorous diffusion and antimony implant. The I-V characteristics of PD4 and SBE5 are shown in Figure 3.1

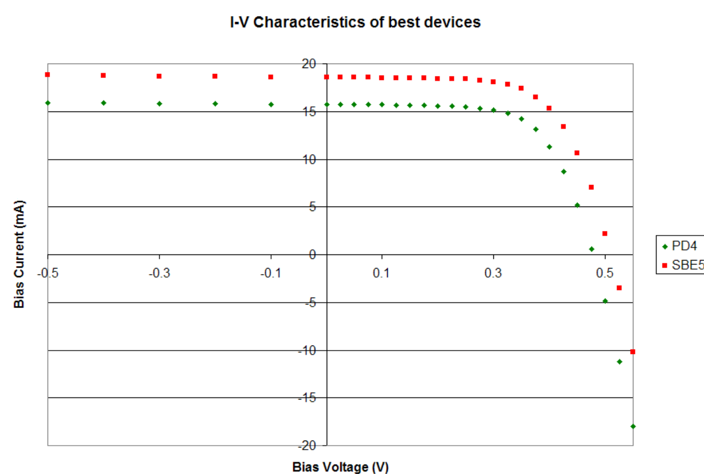

Figure 3.1 I-V characteristics of PD4 (phosphorous) and SBE5 (antimony)

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Fill factors are 65 for both devices. Open circuit voltage of 511 mV for SBE5 and 484 mV for PD4 are on par with what is predicted by the literature. Short circuit current densities of 20 mA /cm2 found from quantum efficiency (QE) measurements are also reasonable [3]. Figure 3.2 shows relative QE measurements for representative examples of all three types of substrates. Note that the QE curves of higher lifetime devices are shifted to the right.

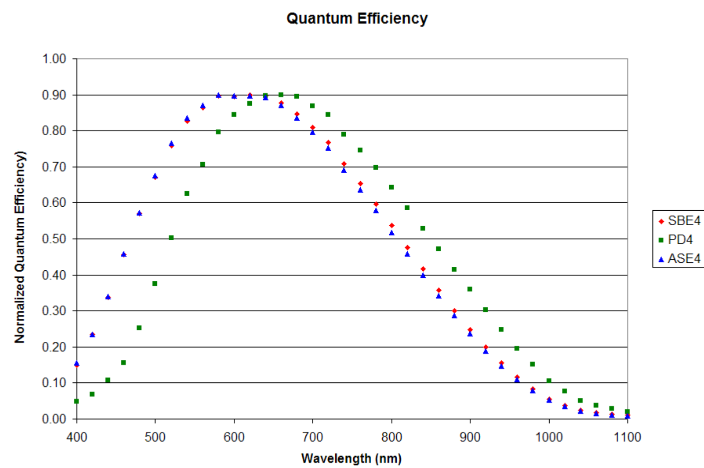

Figure 3.2 QE measurements

While the above devices work well as solar cells, the purpose of constructing devices is to measure the diffusion length and the effective minority carrier lifetime that result from the ion implant. Minority carrier lifetimes of the bare wafer slices are measured by photoconductance, but improvement in device performance needs to be measured and verified by proven techniques. The first of these techniques is QE as described in the methodology chapter. Diffusion lengths for three sets of devices are shown if Figure 3.3. (QE data for remaining devices is found in Appendix V)

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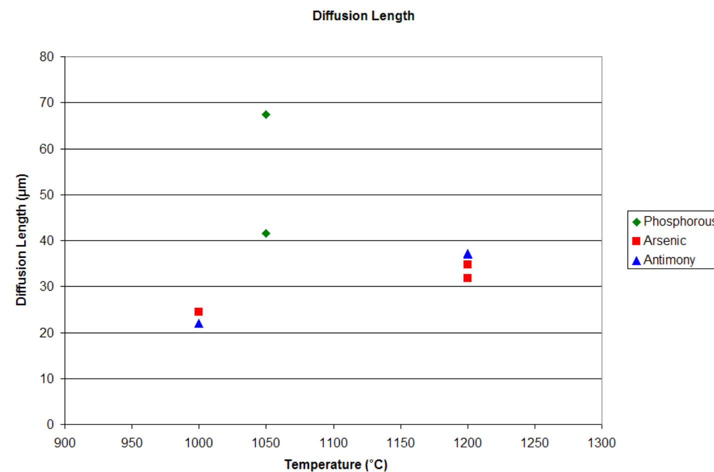

Figure 3.3 Diffusion length vs. temperature

These devices are selected as matched sets to show the effect of annealing temperature on different implant species. The diffusion length for D3 shows arsenic implantation giving a greater diffusion length than antimony. This is true for an annealing temperature of 1000 °C. Devices from wafer E4 show diffusion lengths measured in slices annealed at 1200 °C. Note that antimony and arsenic slices exchange roles; arsenic now has a shorter diffusion length. These sets are representation of temperature extremes used in the annealing experiments. Finally, wafer E5 has a temperature profile that is between wafers E4 and D3. The temperature is ramped from 600 to 1200 °C; as soon as 1200 °C is reached, the tube is cooled. Note that the diffusion lengths are nearly the same with the antimony diffusion length being slightly longer than that of arsenic. Plots of 1/QE vs. 1/α for wafers D3, E4, and E5 are shown in Figure 3.4. Diffusion length is determined from these plots by the reciprocal of the slope of the curves.

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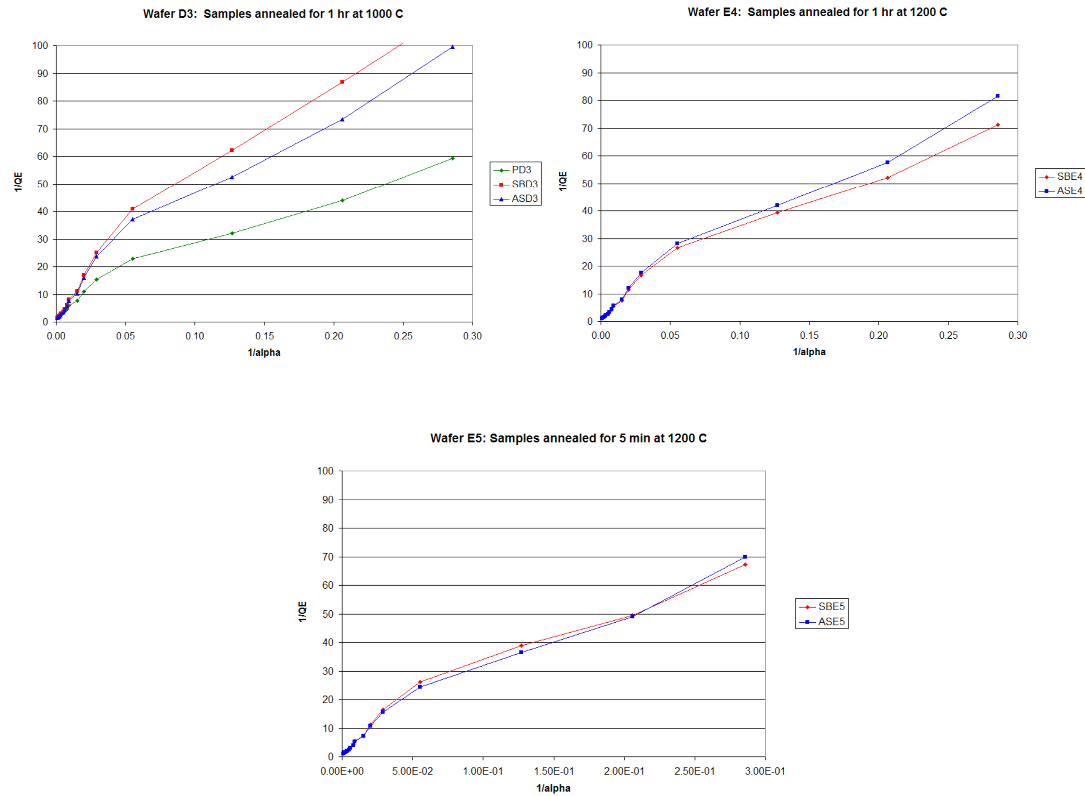

Figure 3.4 Diffusion length data

Carrier lifetimes are observed by RRT as discussed in the methodology section (Figure 3.5). Carrier lifetimes are plotted versus annealing temperature for the all of the devices listed above. The same trends are observed as with the diffusion length measurements. Arsenic devices demonstrate performance superior to antimony devices for lower annealing temperatures and the roles of the two species are reversed at higher annealing temperatures (See Appendix IV for sample RRT data).

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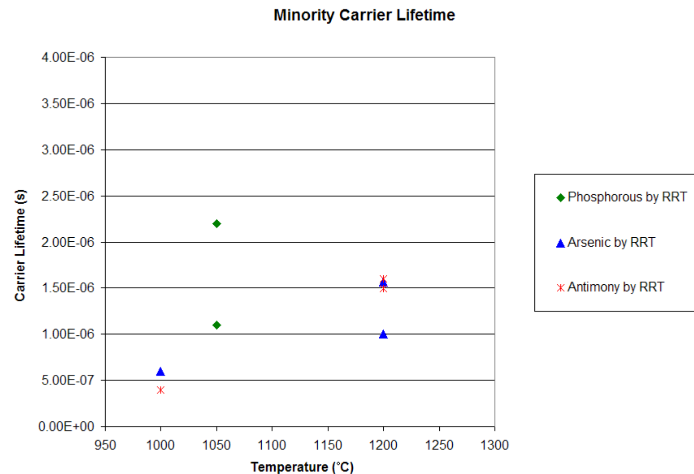

Figure 3.5 Carrier lifetimes versus temperature by RRT

Wafer Slice Data

The results of both implanted species show promise in improving minority carrier lifetime from the initial lifetime of the unprocessed wafer slice. Figure 3.6 shows peak minority carrier lifetime versus minority carrier concentration for all unprocessed wafers. This is as measured by the Sinton WCT-120. Carrier lifetime reported without injection level is not useful as carrier lifetime has been seen to be dependant on injection level (See Appendix III). Therefore all Sinton measurements in this work will either directly report the carrier level or combine it with the lifetime.

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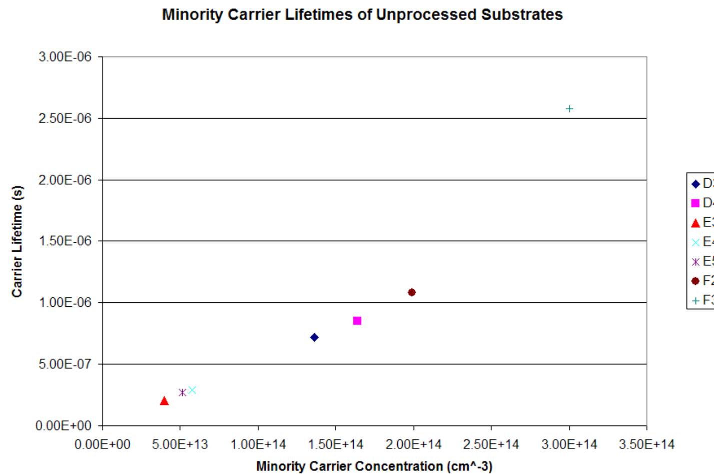

Figure 3.6 Peak minority carrier lifetime versus minority carrier injection level

These data provide a baseline for comparison of the various implantation techniques. From this plot, it is readily apparent that the F series wafers have a much greater minority carrier lifetime that any of the other three series (about three times).

Minority carrier lifetimes for samples D3 through F3 are shown in Figure 3.7 for baseline and both arsenic and antimony implants. Table 3.1 is provided so that device designations can be matched to annealing temperatures. Both the arsenic sample and antimony sample for each wafer type are annealed together for a variety of temperature profiles. The purpose of keeping these samples together is to eliminate the effects of possible furnace tube contamination and variations in cleaning solutions on lifetime. While each set of samples E3 through F3 were processed at the same time, samples D3 and D4 had each implant species annealed separately.

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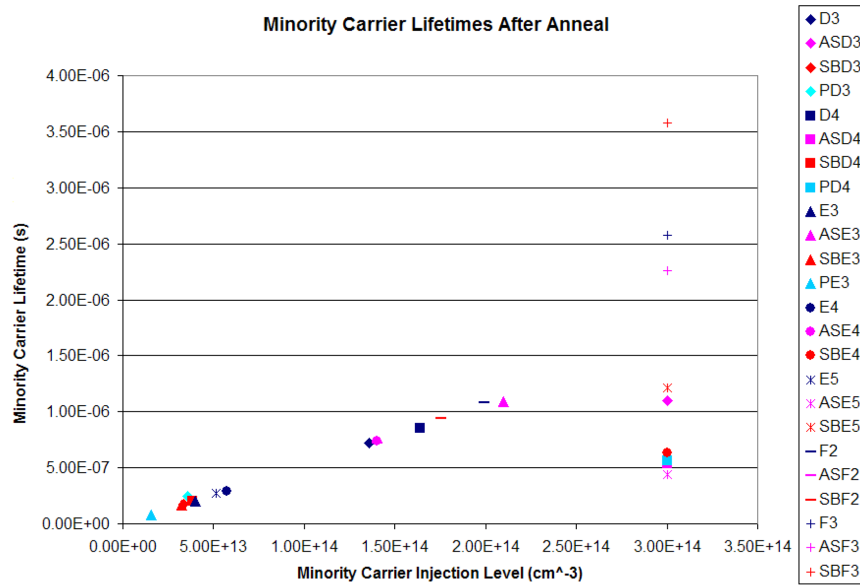

Figure 3.7 Peak minority carrier lifetime versus minority carrier injection level for samples D3 through F3

Table 3.1

Device Designation	Dopant Species	Anneal Temperature (℃)	Time (hr)
PD3	Phosphorous	1050	5
ASD3	Arsenic	1000	1
SBD3	Antimony	1000	1
PD4	Phosphorous	1050	5
ASD4	Arsenic	1100	1
SBD4	Antimony	1100	1
PE3	Phosphorous	1000	1
ASE3	Arsenic	1000	1
SBE3	Antimony	1000	1
ASE4	Arsenic	1200	1
SBE4	Antimony	1200	1
ASE5	Arsenic	1200	0.08333
SBE5	Antimony	1200	0.08333
ASF2	Arsenic	1200	1
SBF2	Antimony	1200	1
ASF3	Arsenic	1250	1
SBF3	Antimony	1250	1

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Figure 3.8 shows the temperature profiles used for the annealing experiments. Generally, 1000 °C is considered safe for crystalline silicon, so the first experiment is to vary the temperature from 600 °C to 1000 °C over the course of an hour. More aggressive profiles are also used, one of which brings the temperature to 1250 °C which is the maximum operating temperature of the furnace tube. Figure 3.9 shows minority carrier lifetime versus annealing temperature as measured by the Sinton WCT-120. The carrier lifetime is reported as carrier lifetime multiplied by injection level.

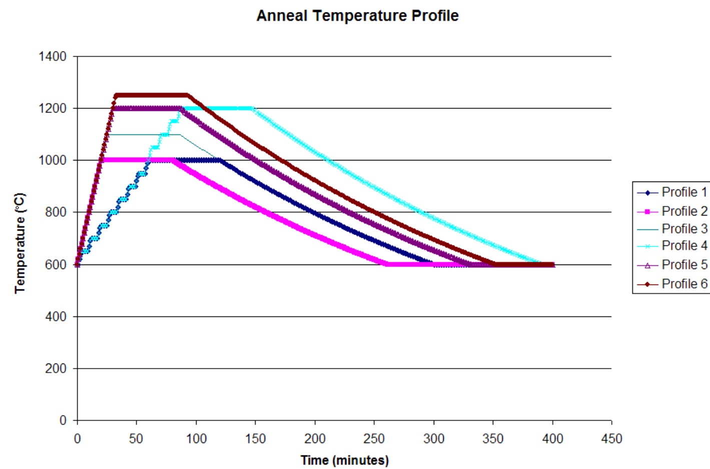

Figure 3.8 Temperature versus time profiles

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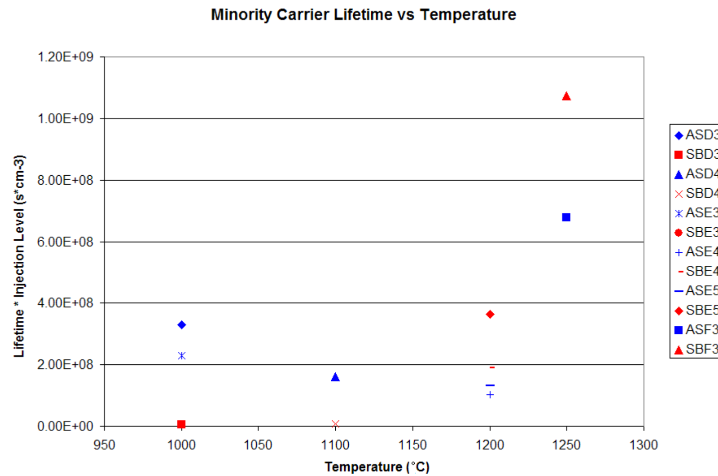

Figure 3.9 Minority carrier lifetime versus temperature by Sinton WCT-120

(Red points represent antimony, blue represent arsenic.)

Initial results suggest both arsenic and antimony species are capable of improvement in carrier lifetime. Arsenic benefits primarily from an annealing profile where temperature is held near 1000 °C for an hour or more. Temperatures greater than 1000 °C appear to improve minority carrier lifetime in arsenic. Antimony implanted samples benefit from temperature profiles where the maximum temperature meets or exceeds 1200 °C. Annealing profiles with temperatures less than 1200 °C do little to improve carrier lifetime as seen in antimony samples SbD3 and SbD4.

Devices C2 and C3 are used to test metallizing techniques once the mesa etch technique proved to be successful. Aluminum is deposited on C2 and C3 and is patterned with chemical etch. The I-V characteristics of both devices are measured under one sun light intensity. Figure 3.10 shows the results of these measurements.

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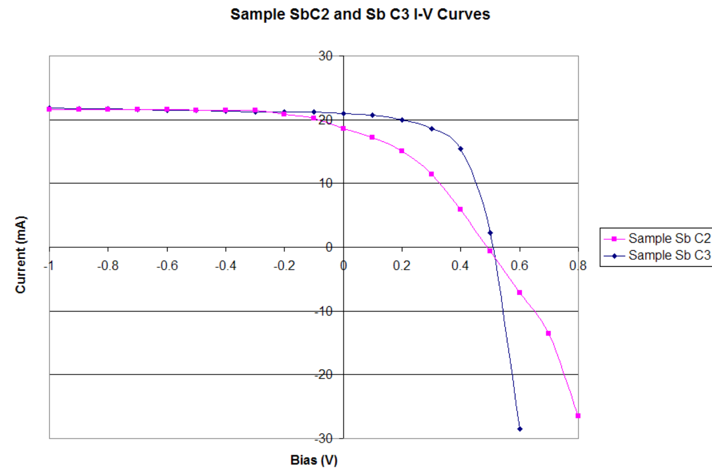

Figure 3.10 I-V Characteristics of samples C2 and C3 before sintering

Sample C3 is placed in a sintering tube at 400 °C. The sample is destroyed due to a power electronics failure that caused the tube to overheat. Sample C2 is placed in a spare tube at 400 °C for a period of 1 hour. I-V characteristics are re-measured and the results plotted in Figure 3.11.

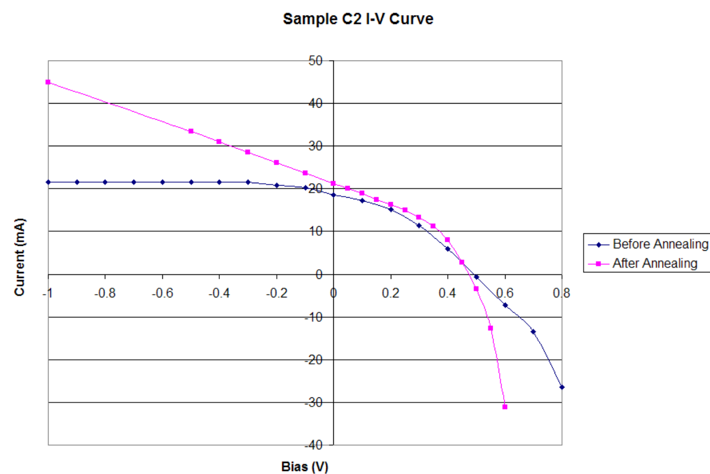

Figure 3.11 I-V characteristics of sample C2 before and after annealing

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The fill factor of sample C2 is clearly improved by the annealing. However this improvement is mitigated by a significant decrease in shunt resistance. Shunt resistance is later shown to be a problem for several devices.

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Chapter 4: Analysis

Material Comparison

As seen in the last section, lifetime and diffusion length data from the devices show that the ion implantation of arsenic and antimony were less successful than phosphorous diffusion for gettering impurities. Antimony implants outperform arsenic implants for higher anneal temperatures, but not at lower temperatures. The best overall solar cell devices were made with phosphorous and antimony.

Looking purely at the data from the Sinton apparatus, it is apparent that both phosphorous diffusion and ion implantation getter impurities after appropriate annealing steps are completed. Conventional wisdom proclaims that it is necessary to anneal substrates after ion implantation in order to repair crystal lattice damage. After a review of the literature, it is not clear that repairing all of the lattice damage is desired. In fact Siedel et. al. [2] found a strong correlation between lattice damage caused by defects and the gettering capability of the implant species.

The assumption that some amount of lattice damage allows impurities to be trapped explains why the performance of arsenic implantation as a getter degraded with increasing anneal temperature. Since there is no overlap between optimal annealing temperatures for arsenic and antimony, it is hard to be sure which causes more lattice damage using the data collected for this work. It is likely that the antimony causes the most damage as temperatures high enough to cause lifetime degradation in antimony implanted samples were never reached in this series of experiments.

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If the implant atoms were treated as macroscale objects, then it is logical that the antimony should cause the most lattice damage as antimony has greater mass than arsenic. Momentum is always conserved and is given by Equation 4.1.

$$v_1^{'}m_1^{'} + v_2^{'}m_2^{'} = v_1 m_1 + v_2 m_2 \tag{4.1}$$

where the primes indicate initial quantities, m indicates mass, and v is velocity. Assume that m_1' and v_1' are the mass and initial velocity of the implanted atom and m_2' and v_2' are the initial mass and velocity of the crystal lattice. Let kinetic energy be described by $KE = \frac{1}{2}mv^2$. If this expression is solved for velocity and substituted into Equation 4.1 the result is momentum dependant on the mass of the implant species as shown in Equation 4.2.

$$\sqrt{m_1^{'}} \cdot \sqrt{2KE_1^{'}} + v_2^{'}m_2^{'} = v_1 m_1 + v_2 m \tag{4.2}$$

From this analysis, it is no surprise to see that antimony implanted substrates could withstand higher anneal temperature and produce good lifetimes as the silicon lattice must suffer a larger change in momentum with an implant species of higher mass. This assumes that KE is constant.

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Despite not having good agreement between the lifetimes measured by the Sinton WCT-120 and the other two carrier lifetime measurement techniques, the trends shown by both techniques are similar. That is, the lifetimes of arsenic implants are better than those of antimony implants at low temperatures and the roles are reversed at higher temperatures. As mentioned earlier, the Sinton apparatus was not used after the contact metallization due to the low signal to noise ratio that would result from the metal surface having such a high conductance compared to the silicon.

To explain discrepancies between the Sinton apparatus and the device measurement techniques, consideration must be given to what each technique is actually measuring. The Sinton apparatus is designed and engineered to measure the effective carrier lifetime of wafers, not devices, at an industrial scale. Eddy currents created by the time varying magnetic field of the RF coil will primarily flow parallel to the pn junction as shown in Figure 4.1.

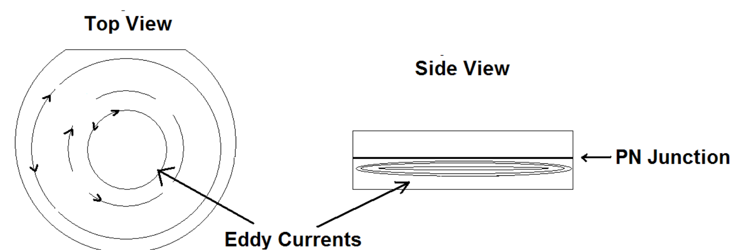

Figure 4.1 Eddy currents from Sinton apparatus

RRT and QE measurement measure the current that flows through the junction and are only concerned with the current that flows through the junction and metallurgical

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contacts. Consider also that the area of the finished devices does not encompass the whole wafer slice, but only a 1.56cm^2 portion of the wafer slice. Since the majority of the silicon surface is removed during the device defining etch, it is quite probable that many lifetime damaging defects were also removed. In any case, the Sinton apparatus appears to work well for what it is designed to do.

Device Comparison

Measurements of the devices made in this work are compared to a heterojunction intrinsic thin layer (HIT) solar cell made on a UMG wafer slice. The slice used was an E series wafer so the diffusion length and RRT data of this device is compared to devices made on the E4 wafer as this wafer is the closest match to that used for the HIT cell. In principle, a HIT cell overcomes wafer impurities by engineering strong electric fields near the active junction to give enough energy to excitons to allow them to jump out of traps without recombination. Figure 4.2 gives the generic device structure and energy band diagram for a HIT solar cell.

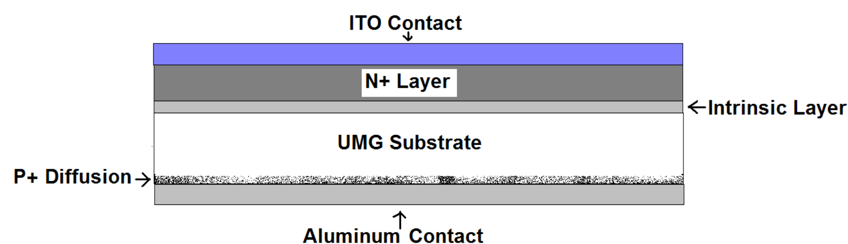

Figure 4.2 HIT solar cell

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What is important with this comparison is that no gettering technique was performed on the slice used for the substrate of this device. The N+ and I layers were grown using chemical vapor deposition techniques. The P+ layer on the bottom is diffused with boron at a high concentration (10^{19} cm^{-3}). Contact is made to the top with indium tin oxide (ITO) and contact is made to the bottom with aluminum [14].

Quantum efficiency, reflection, and RRT measurements for this device are shown Figure 4.3, 4.4, and 4.5 respectively.

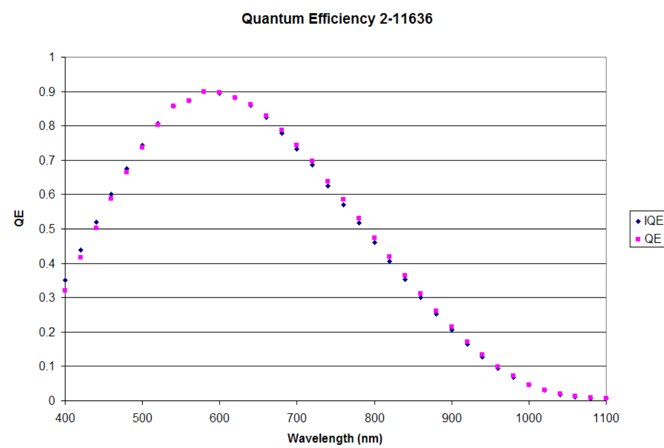

Figure 4.3 Quantum efficiency (Internal and external)

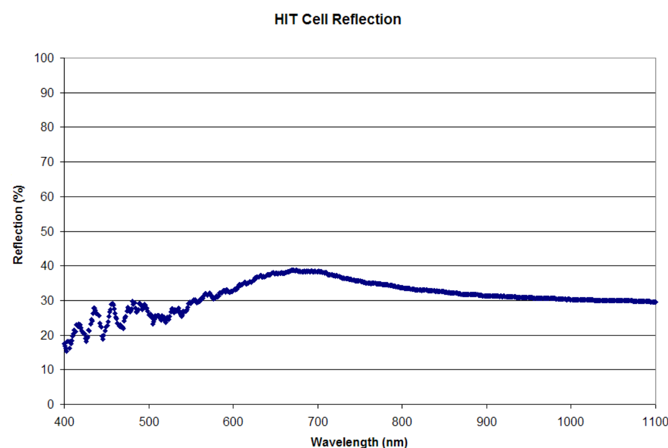

Figure 4.4 Reflection

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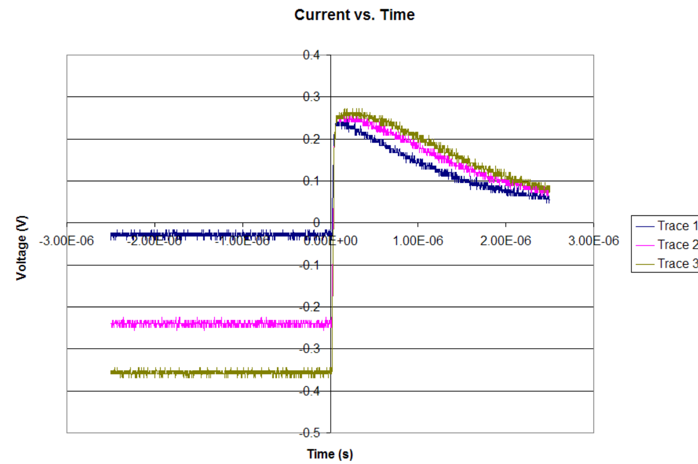

Figure 4.5 RRT current vs. time plots

Diffusion length and minority carrier lifetime are calculated from these measurements in the same manner as the ion implanted devices. The results of these measurements are given in Table 4.1.

Table 4.1

	HIT cell E series wafer	Antimony implant E series wafer
RRT	500 ns	1500 ns
Diffusion Length	19 µm	37.5 µm
Fill Factor	44	58

It is blatantly obvious by comparison of both carrier lifetime and diffusion length measurements that ion implantation and annealing result in significant improvement.

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Lifetime and diffusion length measurements are in good agreement with each other for both devices. Reflection for the HIT device is significantly smaller (30% vs. 45%) than the ion implanted device due to the ITO contact. The ITO alloy, apart from being a transparent conductor, reduces reflection by matching the index of refraction of air to that of silicon. Considering the advantages of the ITO contact on the HIT cell, the improvement in substrate quality by ion implantation is further emphasized (Fill factor of only 44 for HIT cell vs. 58 for antimony implant).

Device Problems

As mention in Chapter 3, many substrates display unacceptably low shunt resistance (< 500 Ω). What is also interesting is that most of the shorted devices occurred for substrates where the annealing temperature was kept low. This is true for 4 of the 6 implanted C series and D2 wafers. Phosphorous diffusion caused little problems, and all failed phosphorous devices can be attributed to the metallization technique used to define their contacts.

Low shunt resistances for the remaining failed devices can be attributed to the shadowing effect caused by the grain boundaries on the surface of the wafer. Ion implantation is done at oblique incidence and as is demonstrated schematically in Figure 4.6; shadowing will cause regions of no doping along surfaces parallel to the ion beam. Regions parallel to the beam include the side walls of defects at the grain boundary edges.

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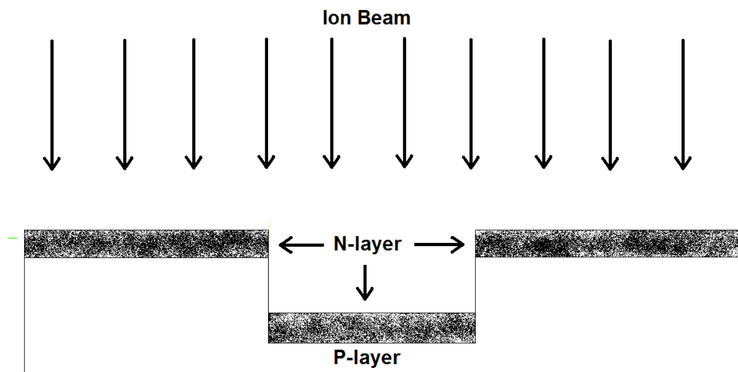

Figure 4.6 Shadowing diagram

Aluminum evaporation is reasonably isotropic and contacts the top surface of the wafer slice as shown in Figure 4.7. After this aluminum is annealed, it makes electrical contact to all surfaces of the silicon and forms a shunt between the N-region and the P-region.

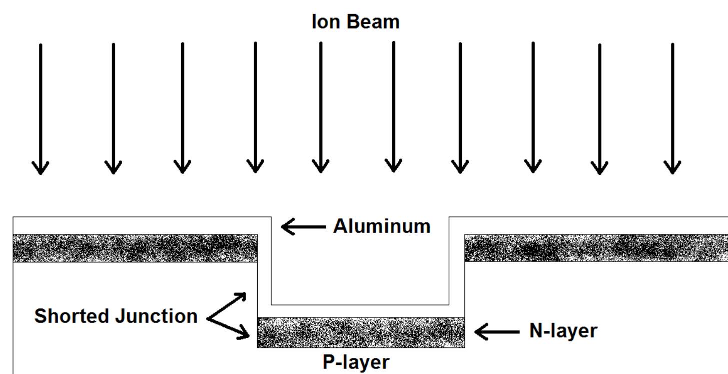

Figure 4.7 Aluminum contact coating

Figure 4.8 shows the average shunt resistance as a function of temperature. Interestingly, as annealing temperature was increased, shunt resistance also increased. This phenomenon can be easily explained; the higher temperature caused the dopants to

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spread out. Voids left by the oblique ion beam are covered by this diffusion. The diffusion coefficients of arsenic and antimony are ten times less than that of phosphorous, thus it was expected for phosphorous to diffuse laterally across the surface more than antimony or arsenic for a given temperature [6].

A definitive test to determine if the angle of the implant is the problem would be to have the implantation repeated at a tilt of some non-zero angle. While the sample is tilted relative to the incidence of the beam, the carousel that holds the wafer slice should also be rotated to guarantee uniform coating of all surface defects. If the shunt resistance of all devices improves then, the cause will be proven correct. Otherwise further investigation is needed.

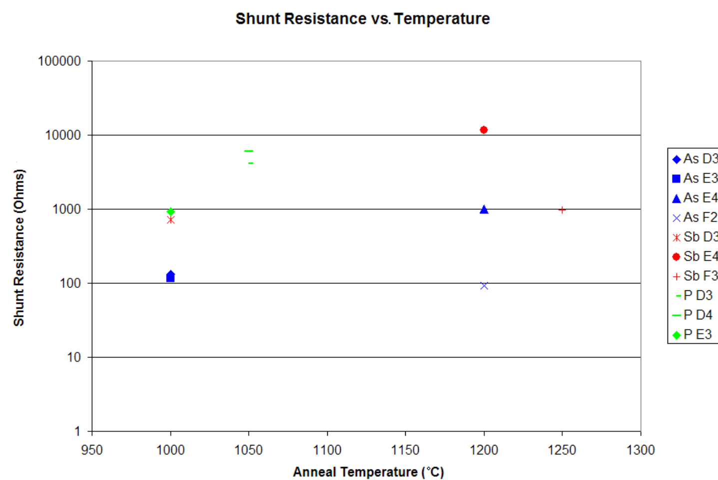

Figure 4.8 Shunt Resistance versus anneal temperature (Arsenic is shown with blue, antimony is shown with red.)

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Wafer Slice Improvement

As is shown in Figure 4.9, the ion implantation techniques performed for this work have improved the effective minority carrier lifetime of the wafer slices by as much as a factor of ten. The plot of Figure 4.9 shows the product of minority carrier lifetime and injection level after processing versus the product of minority carrier lifetime and injection level before processing. Determination of the quantitative improvement is accomplished by dividing the y value by the x value for any particular data point.

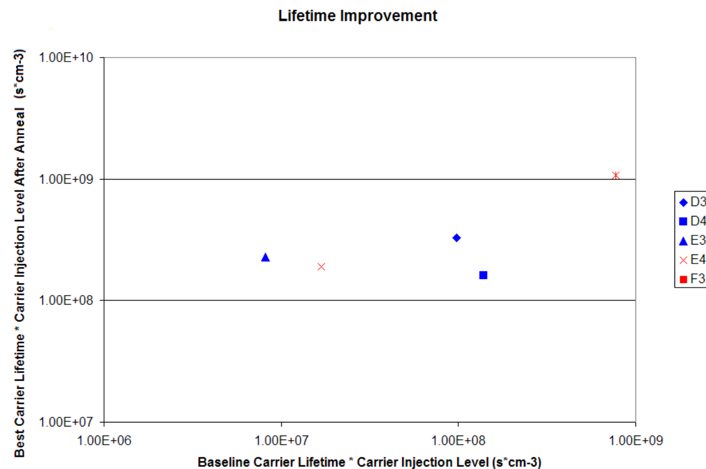

Figure 4.9 Processed minority carrier lifetime * injection level vs. unprocessed minority carrier lifetime * injection level (Arsenic is displayed in blue, antimony is displayed in red.)

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Chapter 5: Conclusion

Ion implantation of both arsenic and antimony both demonstrate the ability to getter impurities from UMG wafers provided the proper annealing technique is used. Even without removal of the gettering layer UMG solar cells with diffusion lengths of at least 20 μm have been produced. When compared with a HIT device made on a similar wafer, a diffusion length improves from 20 to 37.5 μm. Antimony needs more heat than arsenic to realize improvement in substrate lifetimes. Substrates annealed at higher temperatures produce the best devices. The next step is to remove the gettering layer and perform fresh phosphorous diffusions to see if diffusion lengths can be improved further. Future experiments need to be done where ion implant angle is varied such as to assure good coverage. For further research, the implant energy should be increased to see if gettering improves.

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References

1. Wikipedia *Silicon*

2. T. E. Siedel, R. L. Meek, and A. G. Cullis. Direct comparison of ion damage gettering and phosphorous diffusion gettering of Au in Si. Journal of Applied Physics, Vol 46. No 2. February 1975

3. D. Jarwoska and E. Tarnowska. Gettering of Au atoms in Si induced by ion implantation. Journal of Physics D; Applied Physics. Vol 26. Pg 2226-2230. 1993

4. Nam-Hoon Cho, Tae-Hoon Huh, Yoon-Taek Jang, Jae-Sang Ro, Jae-Geun Oh, Kil-Ho Lee, Byung-Jin Cho, and Jong-Choul Kim. Annealing behavior of double MeV implanted Silicon. IEEE. Pgs 661-664. 1997

5. J. Libal, T. Buck, R. Kopecek, P. Fath, K. Wambach, M. Acciarri, S. Benetti, L. J. Geerligs. Properties of N-type multicrystalline silicon: lifetime, gettering, and H-passivation.

6. T. C. Chan, C. C. Mai, Diffusion of boron, phosphorous, arsenic, and antimony into (100) and (111) silicon slices. Proceedings of the IEEE April, 1970. Pg 558

7. S.T. Picraux. Impurity gettering. Sandia National Laboratories, Albuquerque, NM 87185

8. R. Krauss-Rheberg, F. Borner, F. Redmann, J. Gebauer, R. Kogler, R. Kliemann, W. Skorupa, W. Egger, G. Kogel, W. Triftshauser. Identification of getter defects in high energy self implanted silicon at Rp/2. Physica B. Vol 308. Pg 442. 2001

9. Core Systems. Public Documents. Assorted Range Tables. Accessed July 1, 2009

10. G. Tuttle. E E 432 Summer 2008 Lecture Notes. Accessed June 30, 2009

11. P. Reusswig. Measurement of minority carrier lifetimes in nanocrystalline silicon devices using reverse-recovery transient method. Iowa State University, 2008.

12. S. Martinuzzi, O. Palais, M. Pasquenelli, and F. Ferrazza. N-type multicrystalline wafers and rear junction solar cells. European Journal of Applied Physics. Vol. 32. Pg 187. 2005

13. V. Schlosser. Limiting factors for the application of crystalline upgraded metallurgical grade silicon. IEEE Transactions on electron devices Vol. 31 No. 5 May, 1984

14. M. Tanaka, S. Okamoto, S Tsudge, and S. Kiyama. Development of HIT solar cells with more than 21% conversion efficiency and commercialization of highest performance

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HIT modules. Proceedings of 3rd World Conference on Photovoltaic Energy Conversion, 2003. Vol. 1 Pages 955 – 958.

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Appendix I: RCA Standard Clean

The RCA standard clean was developed by the Radio Corporation of America for cleaning the surface of a silicon wafer before any high temperature (T > 400 °C) processing. The purpose of this procedure is to remove all traces of organic and metallic material. Especially any materials that could introduce any deep-level trap states in the silicon. The process is detailed as follows.

I. Prepare the following three solutions
   a. 5:1 DI (18 MΩcm) H_2O:NH_4OH
      i. Heat to 80 °C
      ii. Add 1 part H_2O_2
   b. 6:1 DI H_2O:HCl
      i. Heat to 80 °C
      ii. Add 1 part H_2O_2
   c. 50:1 DI H_2O:HF

II. When solutions have recovered to 80 °C immerse silicon into the base solution (NH_4OH) for 15 min

III. Rinse for 5 min in DI water

IV. Immerse in HF solution for 15 seconds

V. Rinse for 1 min in DI water

VI. Immerse in acid solution (HCl) for 15 minutes

VII. Rinse for 3 min in DI water

VIII. Dry with dry N2 gas.

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Appendix II: Relevant Chemistry

Pyrolytic Wet Oxidation

Pyrolytic wet oxidation consists of burning hydrogen in the presence of oxygen to form steam. For this work a mixture of 6 SLPM of hydrogen and 4 SLPM of oxygen is heated to 800 °C. Combustion is spontaneous and is maintained throughout the oxide growth step.

MIF 300 Developer

MIF 300 Developer is a commercially available dilute mixture of tetramethyl ammonium hydroxide and is used as a developer for acid based photoresist compounds. MIF 300 is an appropriate developer for AZ5214E photoresist.

Buffered Oxide Etch

Buffered oxide etch is a solution of hydrofluoric acid buffered with ammonium fluoride. It is used to aggressively etch silicon dioxide.

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Appendix III: Sinton Control Panel

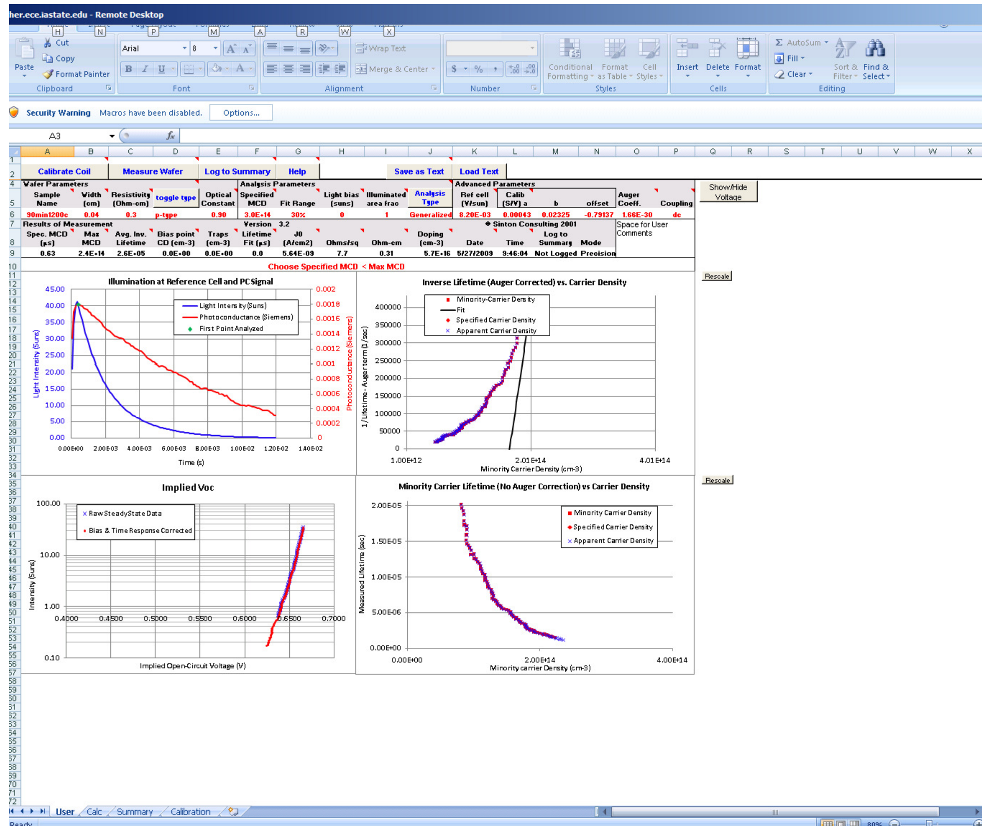

Figure A2.1 Sinton control panel

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Appendix IV: RRT Raw Data

Devices are intentionally biased in such a manner as to have the reverse current be a positive value. This is done to allow oscilloscope curves with ambiguous inflection points to be plotted with the time axis changed to logarithmic scale. Since the decay after the storage time is exponential, it will show up on the log plot as a line with a slope equal to the decay constant of the curve. The inflection point is seen at the beginning of this line. An example is given below in Figure A4.1.

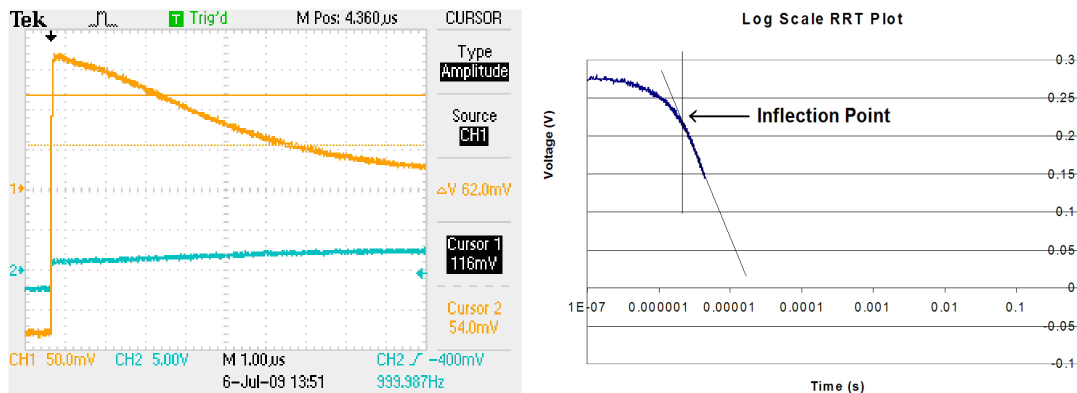

Figure A4.1 Sample RRT curve and inflection extraction technique (SBE4 2nd curve)

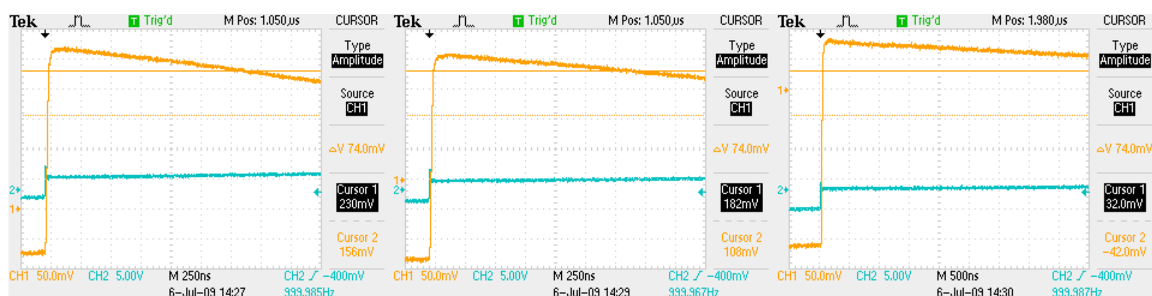

Figure A4.2 PD4

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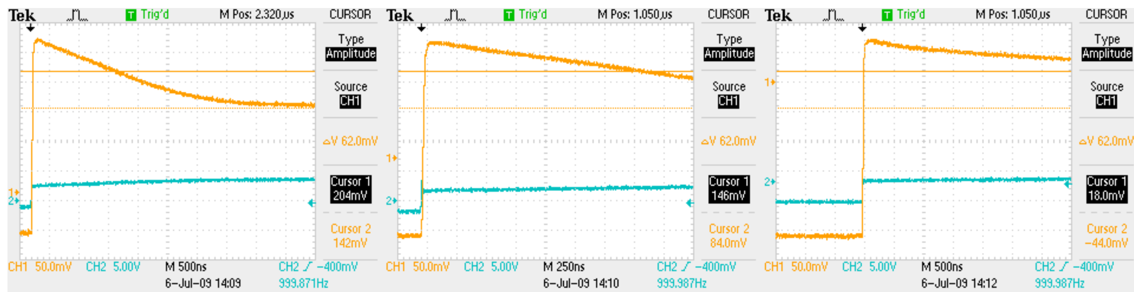

Figure A4.3 ASE5

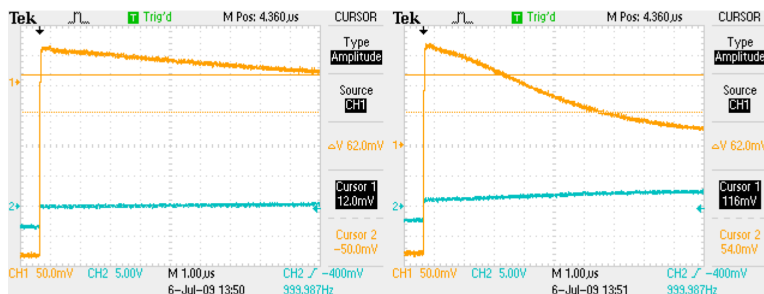

Figure A4.4 SBE4

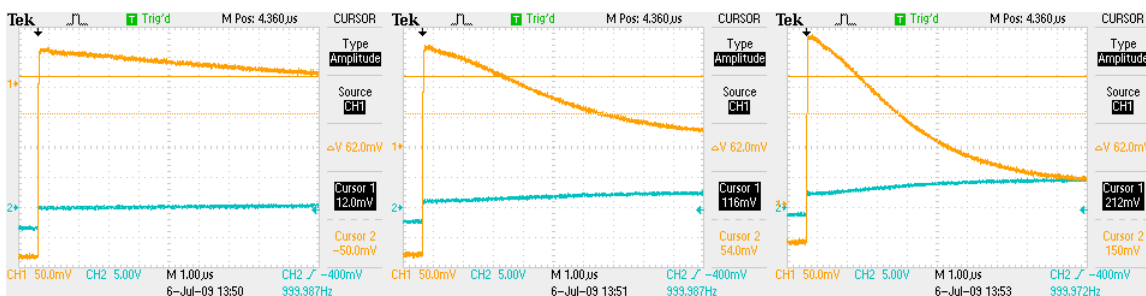

Figure A4.5 SBE5

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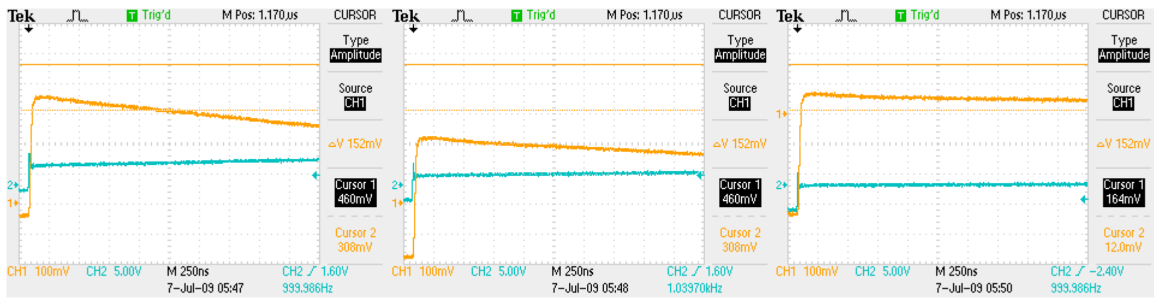

Figure A4.6 ASE4

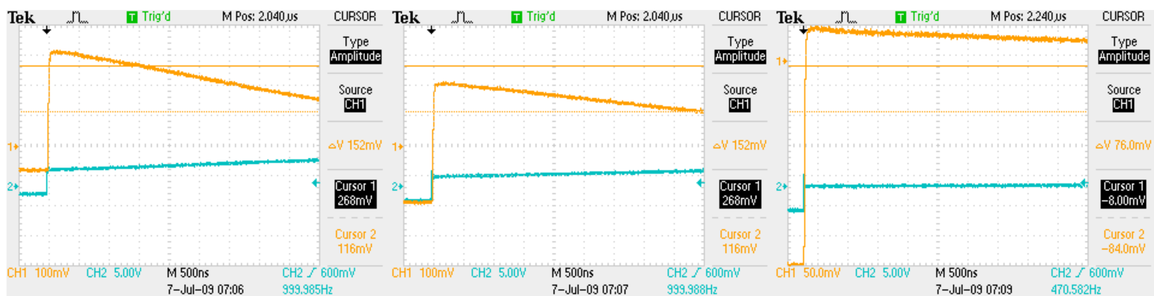

Figure A4.7 PD3

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Appendix V: Optical Data

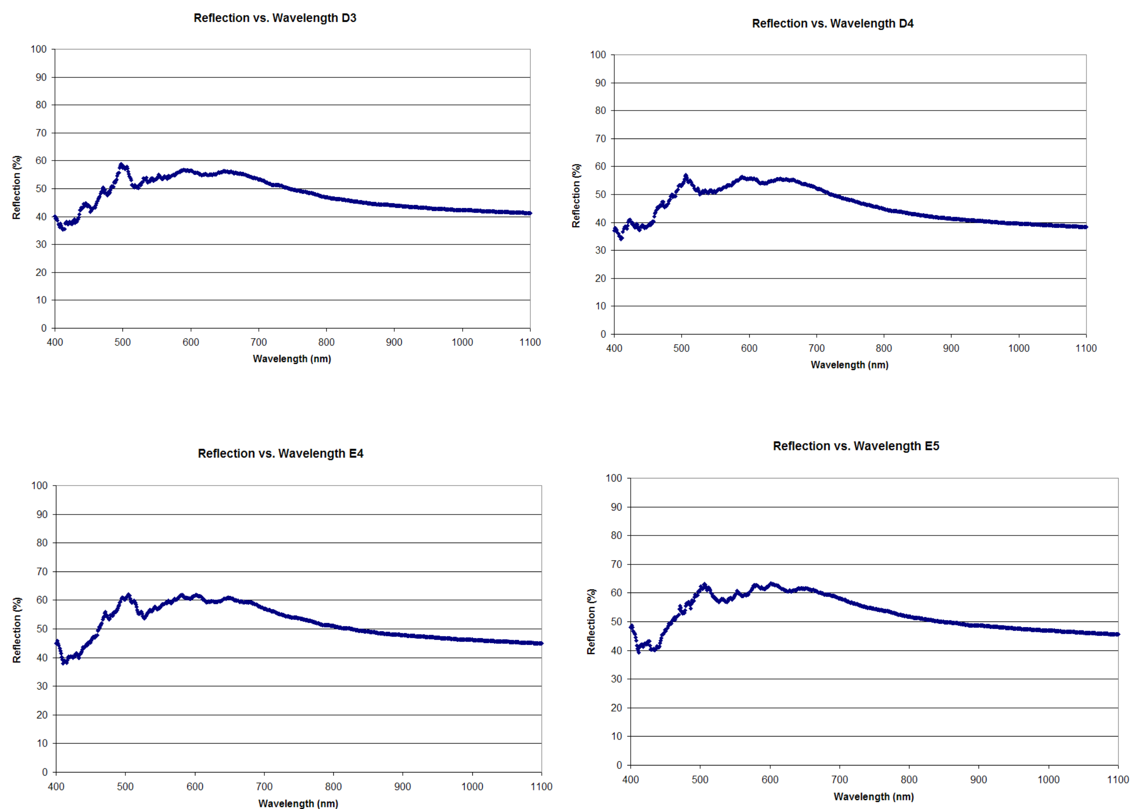

Figure A5.1 Reflection vs. wavelength for device wafers

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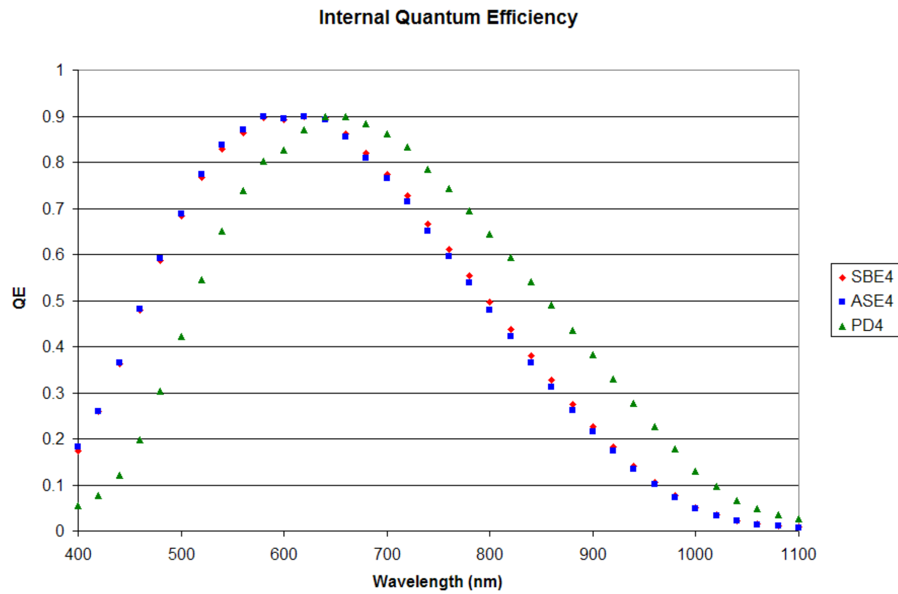

Figure A5.2 Internal QE for devices PD4, ASE4, and SBE4

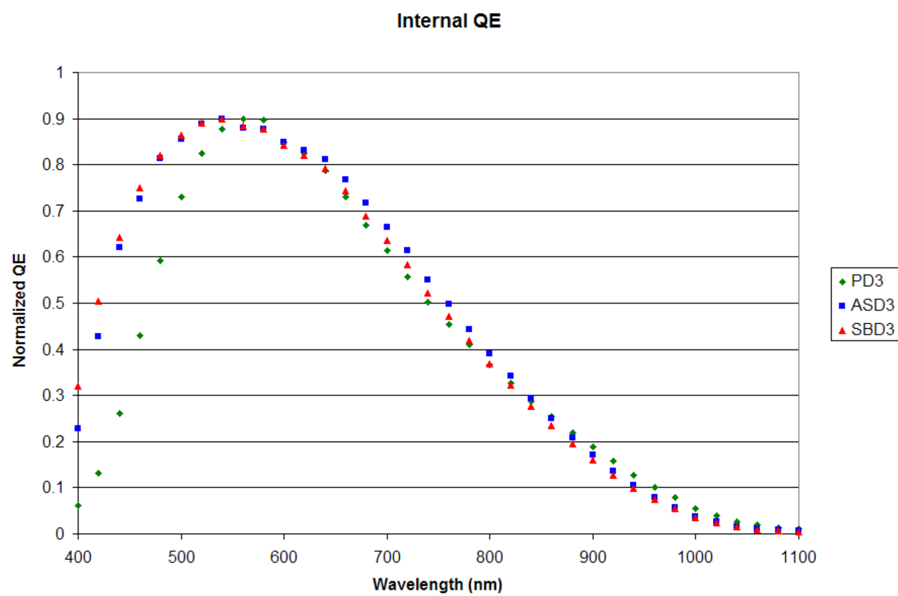

Figure A5.3 Internal QE for devices PD3, ASD3, and SBD3

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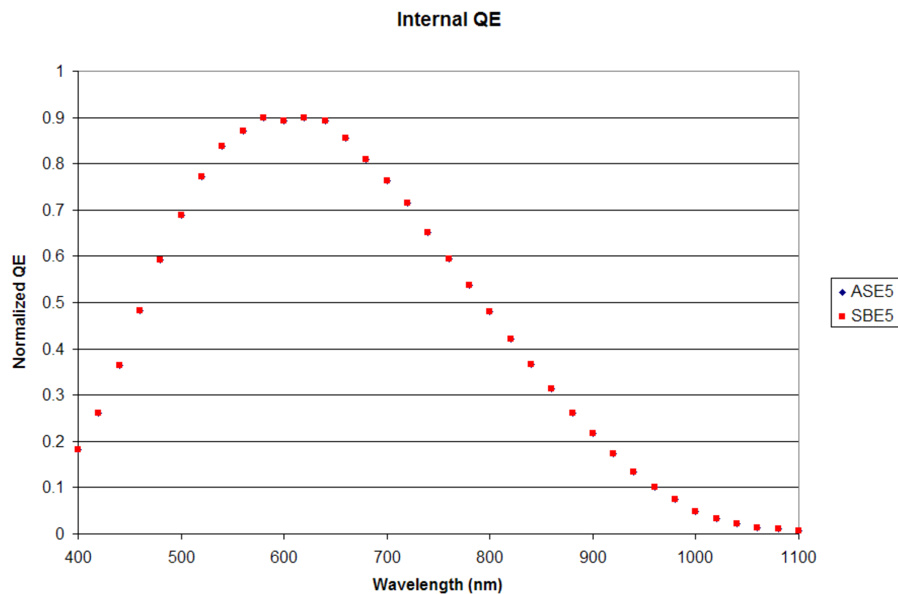

Figure A5.4 Internal QE for devices ASE5 and SBE5

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